

Claims

What is claimed is:

1. A method of fabricating complementary bipolar transistors on a semiconductor wafer, the method comprising the steps of:

5 forming a first electrode corresponding to a first transistor, and a second electrode corresponding to a second transistor which is complementary to the first transistor, the first and second electrodes being formed on an upper surface of the semiconductor wafer;

selectively introducing a first impurity into the first and second electrodes;

forming a third electrode corresponding to the first transistor, the third electrode being self-aligned with and electrically isolated from the first electrode, and forming a fourth electrode corresponding to the second transistor, the fourth electrode being self-aligned with and electrically isolated from the second electrode;

selectively introducing a second impurity into the third and fourth electrodes;

forming a first active region of the first transistor and a first active region of the second transistor, whereby at least a portion of the first impurity associated with the first and second electrodes diffuses into the first active regions of the first and second transistors; and

forming a second active region of the first transistor and a second active region of the second transistor, whereby at least a portion of the second impurity associated with the third and fourth electrodes diffuses into the second active regions of the first and second transistors.

20 2. The method of claim 1, further comprising the step of:

forming a dielectric spacer on a vertical sidewall portion of each of at least the first and second electrodes, the dielectric spacers electrically isolating at least the first and second electrodes from an adjacent structure formed on an upper surface of the semiconductor wafer.

25 3. The method of claim 2, wherein the step of forming the at least one dielectric spacer comprises the steps of:

performing at least one of depositing an oxide layer on the upper surface of the substrate and growing an oxide layer on an upper surface of the semiconductor wafer; and

etching the semiconductor wafer until the oxide layer on a horizontal portion of the semiconductor wafer is substantially removed and the oxide layer substantially remains on the sidewall portions of at least the first and second electrodes.

4. The method of claim 1, wherein the step of forming the first and second electrodes comprises the steps of:

forming a first polysilicon layer on the upper surface of the semiconductor wafer;

forming a hard mask layer on the first polysilicon layer;

selectively patterning the hard mask layer to define predetermined areas of the first polysilicon layer to be etched; and

etching away the predetermined areas of first polysilicon layer.

5. The method of claim 4, wherein the step of forming the first and second electrodes further comprises rapid thermal annealing the semiconductor wafer for substantially removing residual oxide between the first polysilicon layer and the upper surface of the semiconductor wafer.

6. The method of claim 4, wherein the step of forming the third and fourth electrodes comprises the steps of:

forming a second polysilicon layer on the upper surface of the semiconductor wafer;

forming a hard mask layer on the second polysilicon layer;

selectively patterning the hard mask layer to define predetermined areas of the second polysilicon layer to be etched; and

etching away the predetermined areas of the second polysilicon layer.

7. The method of claim 6, wherein the step of forming the third and fourth electrodes further comprises rapid thermal annealing the semiconductor wafer for substantially removing

residual oxide between the second polysilicon layer and an upper surface of the semiconductor wafer.

8. The method of claim 1, wherein the steps of forming the first, second, third and fourth electrodes comprises:

5 forming a first polysilicon layer on the upper surface of the semiconductor wafer;
forming a hard mask layer on the first polysilicon layer;
selectively patterning the hard mask layer to define predetermined areas of the first polysilicon layer to be etched;

etching away the predetermined areas of the first polysilicon layer to form the first and second electrodes;

forming dielectric spacers on vertical sidewall portions of each of the first and second electrodes;

forming a second polysilicon layer on the upper surface of the semiconductor wafer;
performing a blanket etch-back of the semiconductor wafer until at least a portion of each of the dielectric spacers on the sidewalls of the first and second electrodes is detected at an upper surface of the semiconductor wafer;

selectively patterning the second polysilicon layer to define predetermined areas of the second polysilicon layer to be etched; and

etching away the predetermined areas of the second polysilicon layer to form the third and fourth electrodes.

9. The method of claim 1, wherein the step of selectively introducing the first impurity into the first and second electrodes comprises implanting the first and second electrodes with a predetermined concentration of the first impurity.

10. The method of claim 1, further comprising the step of forming a silicide layer on an upper surface of at least one electrode associated with the complementary transistors, the silicide layer providing a substantially low ohmic connection with a corresponding electrode.

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 11. The method of claim 1, further comprising the steps of:
 forming a dielectric layer on the semiconductor wafer such that an upper surface of the semiconductor wafer is substantially planar;
 forming a plurality of contact windows at predetermined areas in the dielectric layer;
 depositing a conductive layer on the upper surface of the semiconductor wafer; and
 selectively patterning the conductive layer to form a plurality of contacts, the contacts being electrically connected to respective electrodes associated with the complementary bipolar transistors.

12. The method of claim 1, wherein the step of selectively introducing the second impurity into the third and fourth electrodes comprises implanting the third and fourth electrodes with a predetermined concentration of the second impurity.

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 13. The method of claim 1, further comprising the step of:
 performing a controlled rapid thermal anneal on the semiconductor wafer, whereby predetermined characteristics of the complementary bipolar transistors are set to a desired value.

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 14. A pair of complementary bipolar transistors formed on a semiconductor substrate, each of the complementary bipolar transistors comprising:
 a collector region, a base region, and an emitter region, the base region having a conductivity type that is complementary to a conductivity type of the collector and emitter regions;
 a collector electrode formed on an upper surface of the semiconductor substrate, the collector electrode being electrically coupled to the collector region; and

a base electrode and an emitter electrode formed on an upper surface of the semiconductor substrate, the base electrode being electrically coupled to the base region and the emitter electrode being electrically coupled to the emitter region;

wherein the base and emitter electrodes of the complementary bipolar transistors are configured such that one of:

(i) the base electrode of a first transistor of the complementary bipolar transistors is self-aligned to and electrically isolated from the emitter electrode of the first transistor, and the emitter electrode of a second transistor of the complementary bipolar transistors is self-aligned to and electrically isolated from the base electrode of the second transistor; and

(ii) the emitter electrode of a first transistor of the complementary bipolar transistors is self-aligned to and electrically isolated from the base electrode of the first transistor, and the base electrode of a second transistor of the complementary bipolar transistors is self-aligned to and electrically isolated from the emitter electrode of the second transistor

15. An integrated circuit including at least one pair of complementary bipolar transistors, each of the transistors in the at least one pair of complementary bipolar transistors comprising:

a collector region, a base region, and an emitter region, the base region having a conductivity type that is complementary to a conductivity type of the collector and emitter regions;

a collector electrode formed on an upper surface of the integrated circuit, the collector electrode being electrically coupled to the collector region; and

a base electrode and an emitter electrode formed on the upper surface of the integrated circuit, the base electrode being electrically coupled to the base region and the emitter electrode being electrically coupled to the emitter region;

wherein the base and emitter electrodes corresponding to at least a given pair of complementary bipolar transistors are configured such that one of:

(i) the base electrode of a first transistor in the given pair of complementary bipolar transistors is self-aligned to and electrically isolated from the emitter electrode of the first transistor,

and the emitter electrode of a second transistor in the given pair of complementary bipolar transistors is self-aligned to and electrically isolated from the base electrode of the second transistor; and

(ii) the emitter electrode of the first transistor in the given pair of complementary bipolar transistors is self-aligned to and electrically isolated from the base electrode of the first transistor, and the base electrode of a second transistor in the given pair of complementary bipolar transistors is self-aligned to and electrically isolated from the emitter electrode of the second transistor.

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